Odax Technologies Inc
www.odaxtechnologies.com

ODAX EDA Research Sensor Board

Datasheet

Product Summary

Research-grade electrodermal activity (EDA) / galvanic skin response (GSR) analog front-end board for low-frequency skin-conductance measurement using two skin-contact electrodes. The board uses a low-leakage transimpedance amplifier, buffered reference and excitation rails, a scaled subtraction output stage, a low-pass output filter, and a precision unity output buffer. The exported `VOUT_JACK` signal is a ground-referenced, zero-based analog voltage intended for a high-impedance ADC or DAQ input. The Version A output scale is centered for useful amplitude around 600 kΩ, 1 MΩ, and 2 MΩbaselines, with approximately 2.5 V output at the 70 kΩnear-full-scale design point.

Product family	EDA Research Grade Analog
SKU / Part number	ODAX-EDA-RB1-100-ASM-R1
Document number	ODAX-EDA-RB1-R1
Revision	R1
Release date	2026-07-06
Status	Released

1 Item Information

Item Identification

Item name	ODAX EDA Research Sensor Board
SKU / Part number	ODAX-EDA-RB1-100-ASM-R1
Document number	ODAX-EDA-RB1-R1
Revision	R1
Status	Released

1.1 Description

The ODAX EDA Research Sensor Board is a compact analog sensor board intended for research prototypes, human-computer interaction studies, psychophysiology experiments, affective computing, biofeedback research, and custom data acquisition systems. It applies a nominal 0.5 V differential excitation through known electrode-series resistance, measures the resulting skin-current magnitude with an LMP7721 transimpedance amplifier (TIA), subtracts the buffered reference, scales the result, low-pass filters the signal, and presents a buffered analog voltage at `VOUT_JACK`.

The output is suitable for relative EDA/GSR response timing, event-locked waveform analysis, and calibrated conductance estimation when board-specific constants and ADC scaling are documented. The board is not a medical device and is not intended for diagnosis, monitoring, treatment, or safety-critical use.

1.2 Key Features

- Single-range exosomatic EDA/GSR analog front end with approximately 70 kΩ near-full-scale output design point.
- Low-leakage TIA core using LMP7721 with guarded sensitive-node layout and BAV199 low-leakage summing-node clamp.
- Buffered reference and excitation rails: nominal $V_{\mathrm{REF}} = 0.700$ V, nominal $V_{\mathrm{EXC}} = 0.200$ V, nominal $\Delta V = 0.500$ V.
- Exported zero-based analog output: `VOUT_JACK` $\approx G_{\mathrm{OUT}}(V_{\mathrm{TIA}} - V_{\mathrm{REF}})$ after the output filter settles.
- Nominal output scale: 0.135 V at 2 MΩ, 0.430 V at 600 kΩ, 1.964 V at 100 kΩ, and 2.500 V at 70 kΩ.
- Approximate cascaded low-frequency -3 dB bandwidth of 6.75 Hz for slow EDA/GSR signals.

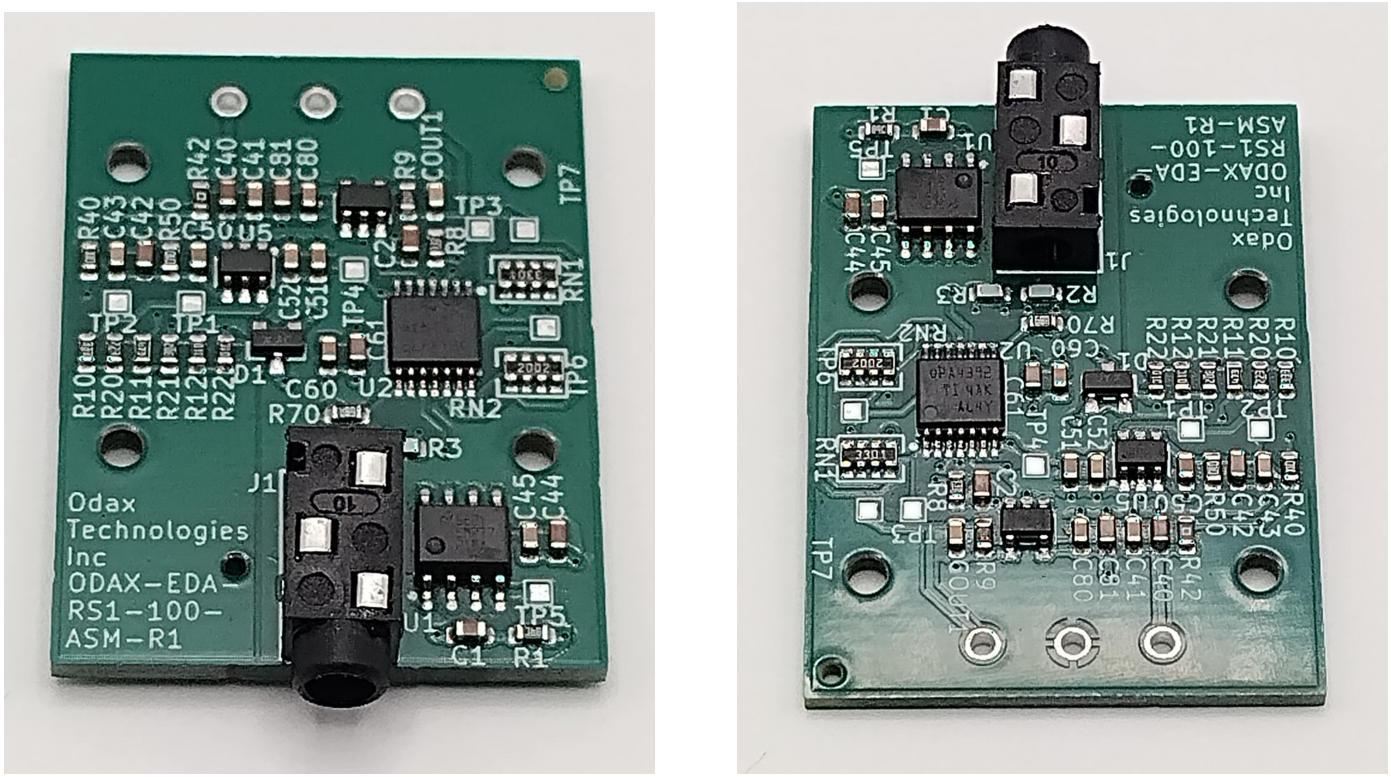
1.3 Applications

- Research EDA/GSR acquisition using a high-impedance ADC or DAQ channel.
- Psychophysiology, HCI, affective computing, biofeedback, and biometric prototyping.
- Wearable or desktop experiments using two finger straps or skin-contact electrodes.
- Firmware and signal-processing development for low-frequency conductance traces.

2 Images and Diagrams

2.1 Product Photos

Figure 1 shows the expected front and back board photographs.



(a) front (b) back

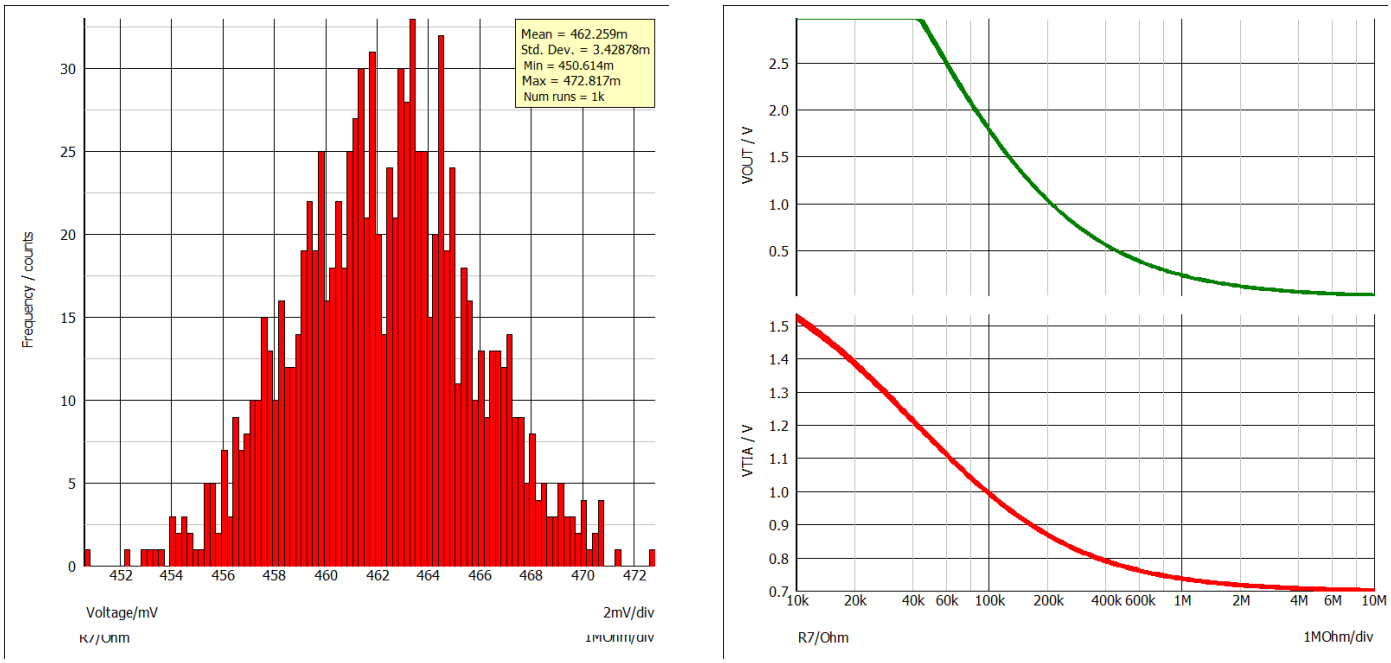
Figure 1: ODAX EDA Research RB1 board photographs.

2.2 Functional Signal Path

Electrodes → LMP7721 TIA → OPA4392 scaled subtraction → R8/C2 output low-pass filter → OPA388 unity output buffer → R9 output isolation → `J2 VOUT_JACK`

2.3 Simulation Results

Figure 2 shows the resistor-simulator output distribution and transfer-curve images supplied with this revision. The histogram image indicates a mean of approximately 462.259 mV, standard deviation of approximately 3.42878 mV, minimum of approximately 450.614 mV, maximum of approximately 472.817 mV, and 1000 runs.



(a) variation histogram

(b) resistor-sweep transfer curve

Figure 2: Supplied simulation images for the Version A output scale.

3 Electrical and Interface Specifications

Unless otherwise stated, values are nominal Version A design values. End-system accuracy depends on resistor tolerance, actual reference and excitation voltages, electrode condition, skin condition, motion, contact pressure, ADC resolution, ADC scaling, ADC input impedance, firmware filtering, and calibration procedure.

3.1 Recommended Operating Conditions and Characteristics

Table 1: Recommended operating conditions and nominal electrical characteristics

Parameter	Symbol	Min	Typ	Max	Notes
Supply voltage, recommended	`PWR_IN`	3.0 V	3.3 V	5.0 V	Use clean battery-powered or isolated low-noise supply while electrodes contact skin.
Preferred ADC supply alignment	-	-	3.3 V	-	For a 3.3 V-only ADC, power the board from the same clean 3.3 V analog domain when practical.
Reference voltage	V_{REF}	-	0.700 V	-	Buffered from REF35125-derived divider.
Excitation voltage	V_{EXC}	-	0.200 V	-	Buffered low-voltage excitation node.
Excitation difference	ΔV	-	0.500 V	-	$\Delta V = V_{\mathrm{REF}} - V_{\mathrm{EXC}}$.
Electrode series resistance	R_{series}	-	40.0 kΩ	-	R2 + R3, included in absolute conversion.
Output gain after TIA	G_{OUT}	-	6.667	-	Ratio set by 100 kΩ/ 15.0 kΩresistor pairs.
Useful signal bandwidth	BW	DC	6.75 Hz	-	Approximate cascaded TIA and output-filter -3 dB bandwidth.
Output response direction	-	-	Positive	-	Higher conductance produces higher `VOUT_JACK`.
ADC input impedance	Z_{ADC}	100 kΩ	Higher	-	High impedance relative to R9 = 100 Ω is preferred.

3.2 Selected Circuit Values

Table 2: Selected Version A electrical values

Circuit area	Value	Description
Reference	U5 = REF35125QDBVR	1.25 V reference feeding the reference/excitation divider.
Reference divider	R10 = 55.0 kΩ, R11 = 50.0 kΩ, R12 = 20.0 kΩ	Nominal V_{REF} = 0.700 V and V_{EXC} = 0.200 V after buffering.
TIA feedback	R1 = 82.5 kΩ, C1 = 180 nF	TIA current-to-voltage conversion and feedback pole.
Electrode series path	R2 = 20.0 kΩ, R3 = 20.0 kΩ	Nominal 40.0 kΩ series resistance in the absolute model.
Scaled subtraction	RN1A = 15.0 kΩ, RN1B = 100 kΩ, RN1C = 15.0 kΩ, RN1D = 100 kΩ	Nominal G_{OUT} = 6.667. Use precision ratio-matched values where practical.
Output filter	R8 = 3.3 kΩ, C2 = 4.7 µF	Main output low-pass filter before the OPA388 buffer.
Output interface	U3 = OPA388IDBVR, R9 = 100 Ω, COUT = 1 nF	Unity output buffer, output isolation, and RF/interface filtering.
Guard drive	R70 = 499 Ω	Guard driver output resistor from `GUARD_BUF_OUT` to `GUARD_DRV`.

3.3 Bandwidth and Output Domain

Table 3: Nominal bandwidth-related poles

Pole / estimate	Formula	Nominal	Notes
TIA feedback pole	$1/(2\pi R1C1)$	10.72 Hz	Set by 82.5 kΩ and 180 nF.
Output filter pole	$1/(2\pi R8C2)$	10.26 Hz	Before capacitor tolerance and DC-bias derating.
Cascaded -3 dB estimate	Two-pole estimate	6.75 Hz	Intended for slow EDA/GSR dynamics, not high-speed biopotentials.
Output-interface pole	$1/(2\pi R9COUT)$	1.59 MHz	RF/interface filtering; not part of low-frequency conductance shaping.

Table 4: Nominal output table using Version A constants

R_{skin}	G	V_{TIA} - V_{REF}	`VOUT_JACK`	V_{TIA}	Interpretation
2.000 MΩ	0.500 µS	0.0202 V	0.135 V	0.720 V	Very dry / very low conductance
1.000 MΩ	1.000 µS	0.0397 V	0.264 V	0.740 V	Dry / low conductance
600 kΩ	1.667 µS	0.0645 V	0.430 V	0.764 V	Nominal expected baseline
470 kΩ	2.128 µS	0.0809 V	0.539 V	0.781 V	Moderate low conductance
400 kΩ	2.500 µS	0.0938 V	0.625 V	0.794 V	Moderate conductance
220 kΩ	4.545 µS	0.1587 V	1.058 V	0.859 V	Moderate conductance
100 kΩ	10.00 µS	0.2946 V	1.964 V	0.995 V	Elevated conductance
70 kΩ	14.29 µS	0.3750 V	2.500 V	1.075 V	Near-full-scale design point
50 kΩ	20.00 µS	0.4583 V	3.056 V	1.158 V	Near or beyond 3.0 V output domain
20 kΩ	50.00 µS	0.6875 V	4.583 V	1.388 V	Beyond useful scaled range
10 kΩ	100.0 µS	0.8250 V	5.500 V	1.525 V	Beyond useful scaled range

The 70 kΩ point is the near-full-scale analog design point, not a digital cutoff. Below about 70 kΩ, `VOUT_JACK` can approach or exceed the available output range, especially when the board is powered from 3.0 V or 3.3 V. If the output clips, exact R_{skin} and conductance cannot be recovered from `VOUT_JACK` alone.

4 Conversion and Calibration

4.1 Output Meaning

`VOUT_JACK` is a scaled zero-based analog signal derived from the TIA output. It is not a direct resistance value. For relative response analysis, such as response timing, within-session amplitude changes, or event-locked waveform shape,

the voltage trace can be analyzed directly when the same board and ADC path are used, the output is not clipped, and absolute conductance is not required.

For absolute resistance, absolute conductance, cross-subject comparison, cross-device comparison, or publication-quality calibrated data, use measured board and ADC constants.

4.2 Measured-Constant Conversion

Use measured constants for calibrated conversion:

$$I_{\text{skin}} = \frac{V_{OUT}}{G_{OUT,actual} R_{1,actual}}$$
$$R_{skin} = \frac{\Delta V_{actual}}{I_{\text{skin}}} - R_{series,actual}$$
$$G_S = \frac{1}{R_{skin}}$$
$$G_{\mu S} = 10^6 G_S$$

An equivalent conductance form is:

$$G_S = \frac{I_{\text{skin}}}{\Delta V_{actual} - I_{\text{skin}} R_{series,actual}}.$$

Using nominal Version A constants for quick review only:

$$I_{\text{skin}} = \frac{V_{OUT}}{6.667 \times 82500}$$
$$R_{skin} = \frac{0.500}{I_{\text{skin}}} - 40000$$
$$G_{\mu S} = \frac{1000000}{R_{skin}}.$$

4.3 Per-Board Calibration Record

Table 5: Values to document for calibrated absolute data

Value	Purpose
$R_{1,actual}$	Measured TIA feedback resistance for current conversion.
$R_{2,actual}$ and $R_{3,actual}$	Measured electrode-series resistances.
$R_{series,actual}$	$R_{2,actual} + R_{3,actual}$; included in the resistance model.
$G_{OUT,actual}$	Measured U2D output gain from the scaled subtraction stage.
$V_{REF,actual}$ and $V_{EXC,actual}$	Measured reference and excitation values.
ΔV_{actual}	$V_{REF,actual} - V_{EXC,actual}$.
Difference-amplifier offset	Used for low-level correction if measurable.
Output-buffer offset	Used for output correction if measurable.
ADC scaling, ADC offset, and ADC input impedance	Needed to convert ADC codes into the true output voltage.
Output-load correction through R9	Needed if ADC or DAQ input resistance is not much larger than 100 Ω.

If the ADC input resistance is finite, correct for the divider formed by R9 and the ADC input:

$$V_{ADC} = V_{OUT\_BUF} \frac{R_{ADCin}}{R9 + R_{ADCin}}$$
$$V_{OUT\_BUF} = V_{ADC} \frac{R9 + R_{ADCin}}{R_{ADCin}}.$$

5 User Connections, Wiring, and Layout Notes

5.1 External Connections

Table 6: Board and electrode connections

Connection	Direction / contact	Description
J0 pad 1	Input	`PWR_IN`. DC supply input, 3.0 V to 5.0 V. Clean 3.3 V preferred.
J0 pad 2	Reference	Ground for board and ADC system.
J1 contact 1	Electrode	`E_PLUS`. Electrode drive contact through R2 from V_{EXC}.
J1 contact 2	Electrode	`E_MINUS`. Measurement return contact through R3 to the TIA summing node.
J2 pad 1	Output	`VOUT_JACK`. Ground-referenced analog EDA/GSR output. Connect to a high-impedance ADC input.
J2 pad 2	Reference	Output ground reference.

Do not intentionally connect either electrode contact to ground. The selected electrode wiring uses no shield conductor; use a short twisted pair for `E_PLUS` and `E_MINUS` outside the PCB.

5.2 Selected Net and Pin Notes

Table 7: Condensed selected wiring notes

Area	Net / component	Rule or connection
Power path	`PWR_IN` to `VDDA_TIA`	`PWR_IN` → F1 → `VIN_AFE` → R42 → `VDDA` → R40 → `VDDA_TIA`.
TIA amplifier	U1 LMP7721	Pin 1 to V_{REF}, pin 4 to `VTIA`, pin 6 to `VDDA_TIA`, pin 8 to `TIA_MINUS`. Pins 2 and 7 connect to `GUARD_DRV`; pin 5 remains NC.
Support amplifier	U2 OPA4392PWR	U2A buffers V_{REF}, U2B buffers V_{EXC}, U2C buffers the guard, and U2D implements scaled subtraction.
Reference and clamp	U5 / D1	REF35125 pin 6 is `VRAW`; pin 5 NR is NC. BAV199 common series junction connects to `TIA_MINUS`; outer pins connect to V_{REF}.
Sensitive node	`TIA_MINUS`	Not exposed on a connector, header, solder interface, or external footprint. No shield connection and no direct guard-copper connection.
Guard and output routing	`GUARD_DRV`, `VOUT_JACK`	Guard copper surrounds the sensitive TIA region without shorting to `TIA_MINUS`. Route `VOUT_JACK` away from the guarded input region and place COUT near the output side of R9.

6 Mechanical Information, Setup, and Restrictions

6.1 Mechanical Characteristics

Table 8: Mechanical characteristics

Parameter	Nominal	Unit	Notes
PCB length	38.5	mm	Without input jack
PCB width	29	mm	.
Total length	41	mm	With input jack

6.2 Electrode Placement and Data Quality

Place two skin-contact electrodes or finger straps on adjacent fingers of the same hand. Keep contact pressure comfortable and consistent. Motion, changing strap pressure, inconsistent placement, skin hydration, electrode material, and cable strain can be larger error sources than the analog front end. Allow the signal to settle after attaching electrodes before using the trace for baseline-sensitive analysis.

6.3 ADC and DAQ Notes

Use an ADC or DAQ range compatible with the board supply and expected subject range. `VOUT_JACK` can exceed 0.700 V, so V_{REF} is not an ADC full-scale reference for this exported output. If the board is powered from 3.3 V, the output

domain is 3.3 V-compatible in normal use. If the board is powered from 5.0 V and connected to a 3.3 V-only ADC, add reviewed scaling, clamping, or protection, and include the resulting transfer function in the conversion model.

6.4 Safety-Critical Electrical Restrictions

Use battery power or a properly isolated research system while electrodes contact skin. Do not power the board from a mains adapter while connected to a person. Do not connect the board, electrodes, or attached microcontroller/DAQ to mains-referenced instruments unless the complete system has appropriate isolation designed and verified by a qualified person. Do not drive `VOUT_JACK` from another source. This board is not a medical device and is not intended for diagnosis, monitoring, treatment, or safety-critical use.

7 Revision History

Table 9: Revision history

Revision	Date	Changes
R1	2026-07-06	datasheet created for ODAX EDA Research RB1, Version A 70 kΩ output scale.

8 Legal Notice

Specifications are subject to change without notice. The information in this document is provided to support product evaluation and system design. The user is responsible for validating the complete measurement system, including electrodes, power source, ADC or DAQ path, and an analysis pipeline. No license is granted by implication or otherwise under any patent, copyright, trademark, or other intellectual property right of Odax Technologies Inc.